

IMPLEMENTATION OF FUZZY – ART NETWORK USING VLSI

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Abstract –

The key objective is to present a mixed- mode VLSI implementation of the fuzzy-ART Structures. The proposed cells are composed of the following: current subtract circuit, multiplier/divider and the S-Z shapes circuit. The efficient performance can be achieved by the individual simulation of the new cells and, second, by the implementation of a decision making system that uses the Mamdani inference method and TMF cells as the knowledge base. Minimum and maximum circuits can be used for the implementation of the Mamdani inference method. The computation can be done in analog current mode. The design of Bias Column Peripheral Cell, Fuzzy-ART Array Cells along with the various Fuzzy-ART structures is to be done. The Measurement of “Column Bias” Cells, “Weight Currents” will be done. The results of above will be verified with the standard algorithm.

Keywords—Membership function, VLSI, decision making system, Adaptive resonance theory (ART), hardware implementations.

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I. INTRODUCTION

Adaptive resonance theory (ART) is a well-established neural network frame work developed by Grossberg et al. at the University of Boston, Boston, MA. The ART algorithms are neural categorizers that share some interesting properties. One of these properties is the online learning, that is, each time a new input exemplar is presented to the system, the system knowledge is updated online to incorporate that knowledge; the system learns while it performs. Another interesting property is that the system maintains a generalization capability which is controlled by a tunable vigilance subsystem. There is a vigilance parameter that tunes the coarseness of the established categories. Setting the vigilance parameter to a low value increases the system generalization capability, thus the system tends to form coarser categories. Setting the vigilance parameter to a high value decreases the system generalization, and it tends to form finer categories, thus increasing the number of categories formed for the same set of input data.

ART 1 is architecture capable of learning (in an unsupervised way) recognition codes in response to arbitrary orderings of arbitrarily many and complex binary input patterns. The ART2 architectures do the same but for analog input patterns. ART 3 [Carpenter, 1990] introduces a search process for ART architectures that can robustly cope with sequences of asynchronous analog input patterns in real time. ARTMAP [Carpenter, 1991b] and Fuzzy-time. ARTMAP [Carpenter, 1991b] and Fuzzy-ARTMAP [Carpenter, 1992] can be taught to learn (in a supervised way) predetermined categories of binary and analog input patterns, respectively[1]. This paper focuses only on the Fuzzy-ART architecture. This architecture has a collection of interesting computational properties:

- Self-Scaling

The self-scaling property discovers Self-Scaling: example, if two binary input patterns have M bits set to '1', and all except m of them are at the same location, these two different input patterns can be classified into the same category if m/M is sufficiently small, or as two different categories if m/M is not so small.

- Vigilance or Variable Coarseness

There is a vigilance parameter (ρ) that adjusts the coarseness of the categories that will be formed.

If the vigilance parameter is set close to '1', more attention will be dedicated to distinguishing very similar input patterns and classifying and learning them as belonging to different categories. However, if the vigilance parameter is close to '0', there must be a significant difference between two input patterns for the system to separate them into two different categories.

- **Subset and Superset Direct Access**

Suppose the system has learned two different categories such that one is represented by a binary pixel image that is a subset of the image representing the other. The first is a subset of the second, which is a superset of the first. Under these circumstances, the system can classify a new input pattern as belonging to either the subset or the superset category, depending on global similarity criteria. No restrictions on input orthogonality or linear predictability are needed.

- **Stable Category Learning**

In response to an arbitrary list of binary input patterns, all interconnection weights subject to learning approach limits after a finite number of learning trials. Learning is guaranteed to stabilize, and it does so for a small number of training patterns presentations.

- **Biasing the Network to form New Categories**

When a new pattern arrives, a competition starts between stored patterns to capture it. One of the competing categories is the empty or uncommitted category. There exists a parameter that can bias the tendency of the uncommitted category to initially capture a new pattern, before the vigilance parameter plays any role.

II. FUZZY-ART ALGORITHM

The fuzzy-ART neural network is a clustering self organizing neural network for analog input patterns. Fig.1. represents the architecture of a fuzzy-ART network. The network is composed of an attention subsystem and an orienting or vigilance subsystem. The attention subsystem is composed of two layers. Layer F1 is the input layer. Input patterns $b = (b_1; b_2; \dots; b_N)$ composed of N analog values are presented to the system. F2 is the category layer. The system categorizes each input pattern as belonging to one of the $[y_1; y_2; \dots; y_M]$ categories. The system stores a weight matrix f_{zijg} of analog values that represents the categories learned by the system. Each category y_j is represented by the weight vector z_j composed of N analog values. The

algorithmic flow diagram of the fuzzy-ART operation is depicted in Fig.1(b). Initially all the interconnection weights z_{ij} are set to their maximum analog value “MAX.” When an analog input vector $b = (b_1; b_2; \dots; b_N)$ is applied to the system, each F1 layer cell receives an analog input component $b_i \in [0; \text{MAX}]$. Then, each F2 category computes its “choice function” T_j , which is a measurement of the similarity between the analog input pattern b and the analog weight template $z_j = (z_{1j}; z_{2j}; \dots; z_{Nj})$ stored in category j . $T_j = b \wedge z_j + \alpha_j$ (1) where \wedge is the fuzzy MIN operator defined by $(X \wedge Y)_i = \min(X_i; Y_i)$, $\|X\|_1 = \sum_{i=1}^N X_{ij}$, and α_j is a positive parameter called “choice parameter.” Layer F2 is a winner-takes-all (WTA) competition network. Each j th F2 cell gives an output y_j which is “1” if that cell is receiving the largest T_j input and “0” otherwise. That is $y_j = 1$; if $T_j = \max(T_j)$ $y_j = 0$; otherwise. This way, the F2 layer selects the category J whose stored pattern z^J most closely resembles input pattern b according to the similarity criterion. The original fuzzy-ART algorithm states that if more than one T_j is maximal, the category j with the smallest index is chosen. The different ways of resolving “ties” may result in some cases where the hardware system produce slightly different final categories than the theoretical fuzzy-ART algorithm for the same set of presentations of input patterns. However, this difference does not affect the functional objectives of the neural network categorizer. For the winning category J , the vigilance subsystem checks the condition $\|b - z^J\|_1 \leq \rho$, where $\rho \in [0; 1]$ is the so called vigilance parameter. If the condition is not satisfied, category J is disregarded by forcing $T_J = 0$. Layer F2 will again select the category with maximum T_j , and the vigilance criterion will be checked again. This search continues until a winning category is selected that fulfills the vigilance criterion. When a category J meeting the vigilance criterion is activated, its weights z^J are updated according to the learning rule $z^J(\text{new}) = b \wedge z^J(\text{old})$. This learning rule is known as the fast-learning mode of the fuzzy-ART algorithm. The digital and analog techniques constitute the two existent approaches for the hardware realization of fuzzy system. The features of these techniques make ones more suitable than the other in specific applications.

For the realization of an efficient fuzzy system, it is required that both techniques contemplate in its design the available time for the rule processing, the space to be occupied by the system and the power it must consume. The digital approach has a high degree of programmability, but it requires of an analog-digital and digital-analog converters for the interaction with the physical

variables that the system works with, the system into an array that occupies a considerably great amount of space. The analog arrays count with a higher degree of difficulty to be programmed, but in terms of space occupation they are more effective arrays because of the reduced number of transistors necessary. Analog systems are preferred for its higher processing velocity and its reduced power consumption. Nevertheless, they present certain disadvantages in comparison with the digital systems, the lack of facility to use CAD (Computer Aided Design) tools for its design, and its major sensitivity to noise and distortion.

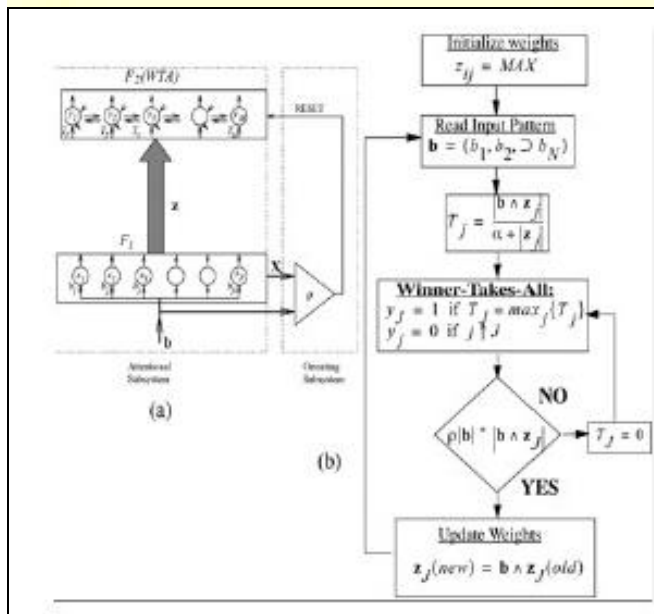


Fig. 1. (a)Topological structure of the fuzzy-ART architecture.

(b) Flow diagram of thefuzzy-ART algorithm.

III. FUZZY-ART CELL DESCRIPTION

A fuzzy-ART cell has to perform the following operations:

- 1) Store an analog weight z_{ij} , which must be initially reset to its maximum analog value “MAX;”vigilance criteria cells.
- 2) Compute the component wise fuzzy-min operation between

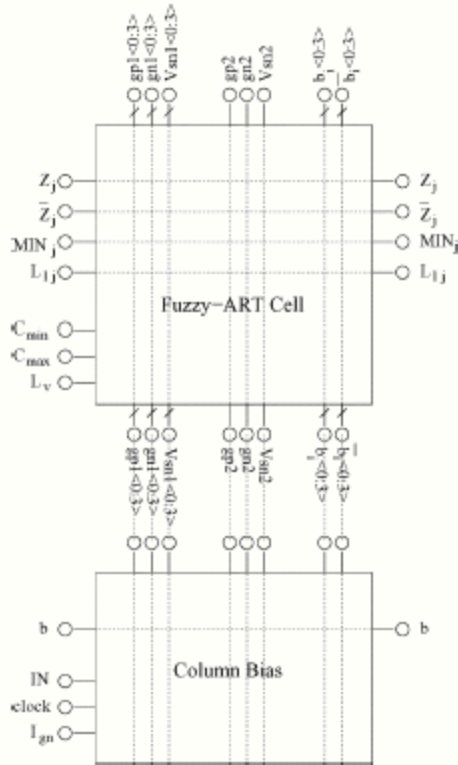


Fig. 2. Block diagram of the connections between the fuzzy-ART cell and the “bias column block.”

the analog stored value z_{ij} and the analog input component b_i ; this analog minimum value will be used in the computation of the choice function T_j and in the evaluation of similarity by the vigilance subsystem;

3) Implement the learning rule; when a category J is selected ($y_J = 1$) that fulfils the vigilance criteria cells.

III. DESIGN ASPECTS OF SUB CELLS

1. Current Subtract Circuit

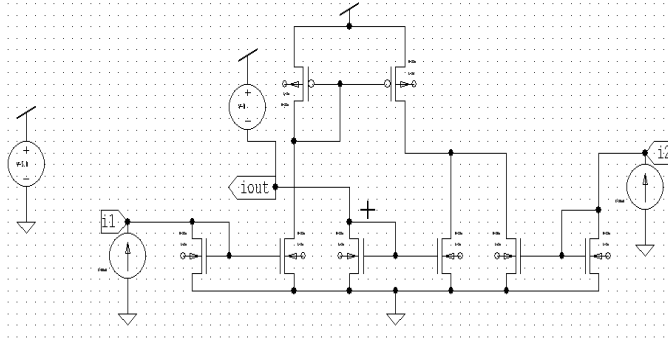


Fig. 3(a) Current Subtract Circuit

The current subtract circuit is shown in Fig. 3(a). This circuit is in the charge of the subtraction of the current I_2 from I_1 . While $I_1 > I_2$ the circuit's output current is the result of the subtraction and when $I_1 < I_2$ the output is equal to zero. The mirror formed by transistor M_1, M_2, M_3, M_4 is in charge of introducing current I_1 into node 4. The result of the subtraction is taken from node 4 by the mirror formed by M_7, M_8 . The mirror is in the charge also preventing the output current from being negative, this is the reason why the output current is equal to zero when $I_1 < I_2$.

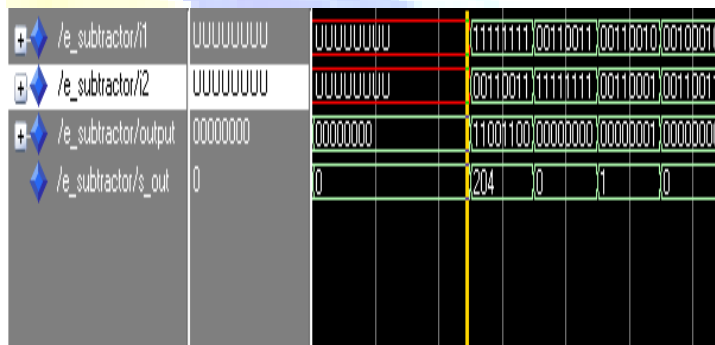


Fig. 3(b) output of Current Subtractor Circuit

Fig. 3(b) shows simulation waveform for Current Subtractor. Here we specify 8 bit input data as data in assigned for i_1 , 8 bit data for i_2 . S_{out} is a 8 bit output signal. Result of subtraction is assigned to s_{out} . When i_1 is greater than i_2 then s_{out} is the subtraction but when i_1 is less than i_2 then s_{out} is zero is shown in fig.

2. Multiplier/Divider

The multiplier/divider circuit is based on the Generalized Tran linear Principle is as shown in Fig. 4(a). Using the Generalized Tran linear Principle we were able to perform the wanted output function using a series of operations. It is based on Kickoff's Voltage Laws.

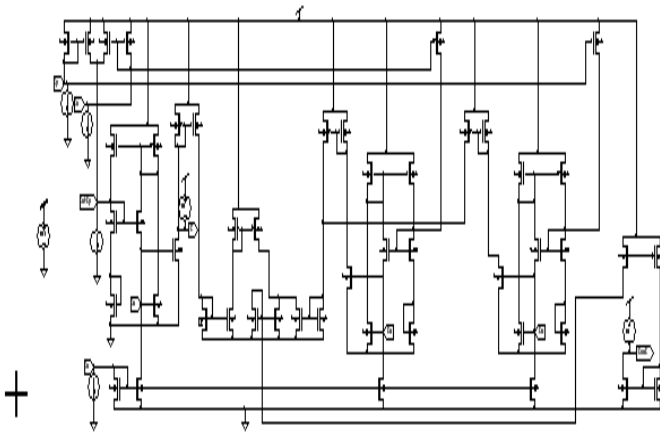


Fig. 4 (a) Multiplier/Divider circuit

Fig. 4(b) shows simulation waveform for multiplier/divider circuit. Here we specify I_x , I_y and I_w are the data input, S-out is the data output. Output of Multiplier/divider is assigned to relation of $I_x I_y / I_w$.

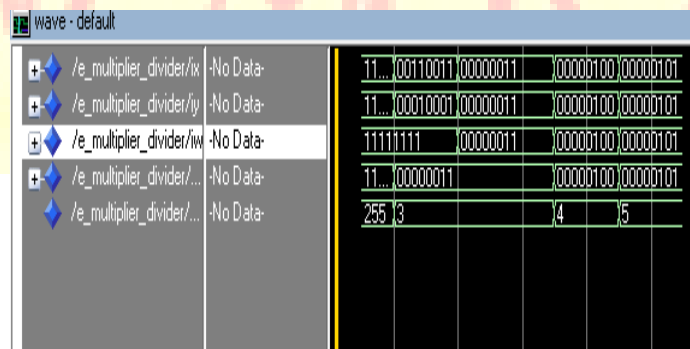


Fig. 4(b) shows the simulation output of the Multiplier/Divider circuit.

3. Circuit for S-Z Shapes

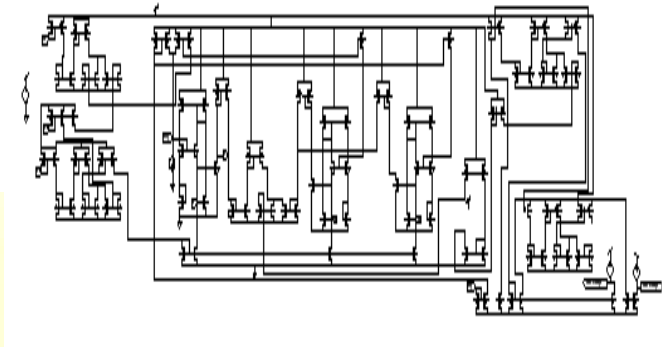


Fig. 5.(a) Circuit for S-Z Shapes

The basic fuzzy cell for the construction of the membership function. This cell delivers in its output S and Z function depending on the input parameter I1, I2.

Figure 5(b) shows the simulation waveform of S-Z. Here we specify i1, i2, i_in, i_amp are the data inputs. s-shape and z-shape are the two outputs. When i_in is greater than i1 and i2 is greater than i_in then s_shape is s_shape and z_shape is z_shape. i_in is greater than i2 then s-shape is i_amp and z-shape is zero. i1 is greater than i_in then s_shape is zero and z_shape is i_amp.

+/e_sz_shapes/i1	01110111	00010001	(11111111)01110111
+/e_sz_shapes/i2	01100110	00110011	(00100010)01100110
+/e_sz_shapes/i_in	01010101	00100010	(01000100)01010101
+/e_sz_shapes/i_amp	01000100	01000100	
+/e_sz_shapes/s_sh...	00000000	00000000	(01000100)00000000
+/e_sz_shapes/z_sh...	01000100	01000100	(00000000)01000100
+/e_sz_shapes/s_nr	00100010	00010001	(10111101)00100010
+/e_sz_shapes/s_dr	00010001	00100010	(11011101)00010001
+/e_sz_shapes/s_divi...	00000010	00000000	(00000010)
+/e_sz_shapes/s_mul...	00000001	00000001	
+/e_sz_shapes/s_sub...	01000100	01000100	
+/e_sz_shapes/s_s_s...	00000000	00000000	
+/e_sz_shapes/s_z_s...	01000100	01000100	

Fig 5(b) Simulation output of Circuit for S-Z

4. TMF Circuit

Fig 6 (a). Shows the schematic that represents the TMF circuit. It is able to generate asymmetric and symmetric membership function. The performance of all the cells that composed TMF circuit.

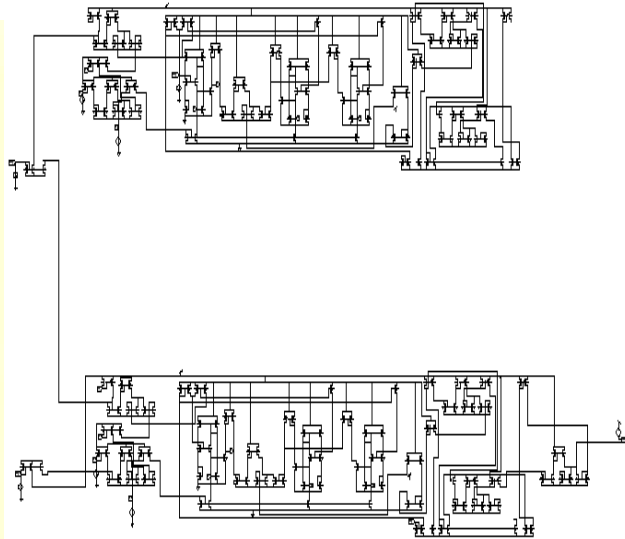


Fig. 6(a) TMF Circuit

Fig. 6(b) shows the simulation waveform of the TMF Circuit. Here we specify the i_{amp} , i_{a_bar} , i_a , i_b , i_c , i_d , i_{in} are the input of TMF Circuit. i_{tmf} is the output of TMF Circuit depending on the input parameter. In other words, the TMF Circuit is formed by two S-Z shapes subcircuit, in combination with a current subtraction.

+ ◆ /e_tmf/i_amp	11111111	11001100
+ ◆ /e_tmf/i_a_bar	11001010	11001010
+ ◆ /e_tmf/i_in	10110011	00110011
+ ◆ /e_tmf/i_a	11001001	11001001
+ ◆ /e_tmf/i_b	00110011	00110011
+ ◆ /e_tmf/i_c	01011101	01011101
+ ◆ /e_tmf/i_d	00110110	00110110
+ ◆ /e_tmf/i_tmf	00000000	00000010
+ ◆ /e_tmf/s_s_shape1	11111111	00000000
+ ◆ /e_tmf/s_z_shape1	00000000	11001100
+ ◆ /e_tmf/s_s_shape2	11001010	00000000
+ ◆ /e_tmf/s_z_shape2	00000000	11001010

Fig 6(b) Simulation output of TMF Circuit

5. Maximum Detection Circuit

The Maximum and minimum Detection circuit are necessary for the implementation of the decision making system based on the mamdani inference method.

A maximum detection circuit with two inputs is shown in Fig. 7(a) as below. This circuit is based on a very simple operation and the cascade connection of various circuit of this kind composes the maximum detection circuit.

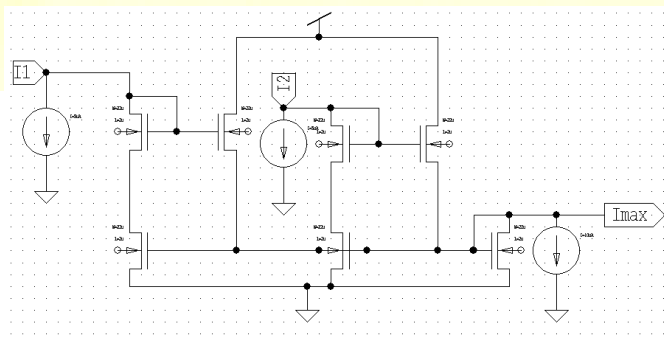


Fig.7 (a) Maximum Detection Circuit with two inputs

6. Minimum Detection Circuit

The minimum detection circuit is obtained as the complement of the maximum of the complements and the circuit is as shown by Fig. 7(b). The minimum detection operator can be implemented by the complement sub-circuits connected to the n inputs and outputs of the maximum detection circuit.

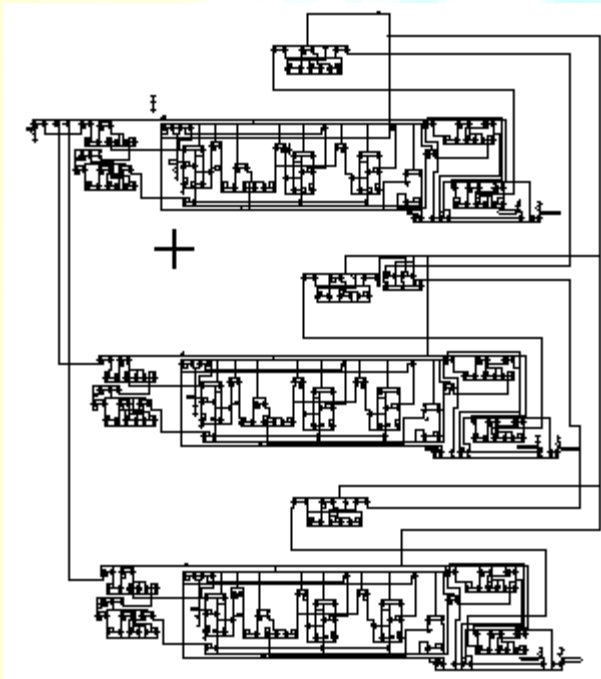


Fig. 7(b) Minimum Detection Circuit

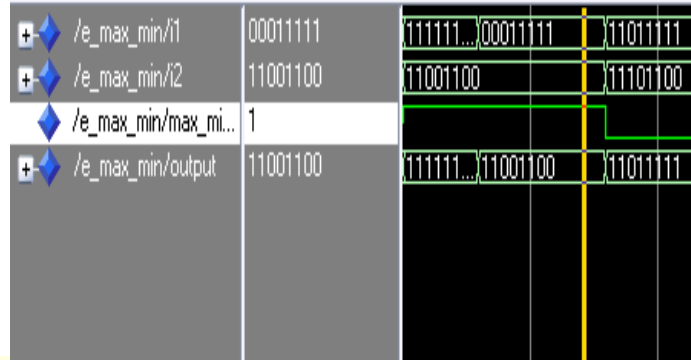


Fig 7(c): Simulation output of Maximum and Minimum Detection Circuit

Fig. 7(c) shows the simulation waveform of maximum and minimum detection circuit. Here we specify the i_1 , i_2 , max_min are the three data inputs and one data out i.e. output. when max_min is assigned to 1, i_1 is greater than i_2 then output is assigned to i_1 . similarly i_2 is greater than i_1 then output is assigned to i_2 . But when max_min is assigned zero value then output shows minimum value.

7. Decision Making System

The cell described in past section will be taken for the implementation of a fuzzy decision making system. This structure is based on a mamdani inference method (MIN-MAX inference).

The mamdani inference method is used commonly for its simplicity and high implementation efficiency, this method is also as MIN-Max inference. It uses the MIN t-norm as the implication function and MAX s-norm as the aggregation operator.

If water temperature and ambient temperature then cold water tap condition

	Water Temperature	Ambient Temperature	Cold Water Tap Condition
1	Cold	Cold	Close a lot
2	Warm	Cold	Close a little
3	Cold	Warm	Close a little
4	Warm	Warm	Do nothing
5	Hot	Cold	Open a little
6	Cold	Hot	Open a little
7	Warm	Hot	Open a little
8	Hot	Hot	Open a lot
9	Hot	Warm	Open a lot

Fig. 8(a) Input-output relationship for the decision making system

This method is an inference mechanism based on based rules of the form:

Rule1: if x1 is A1' and x2 is A2' then y is B'

Rule2: if x1 is A12' and x2 is A22' then y is B'.

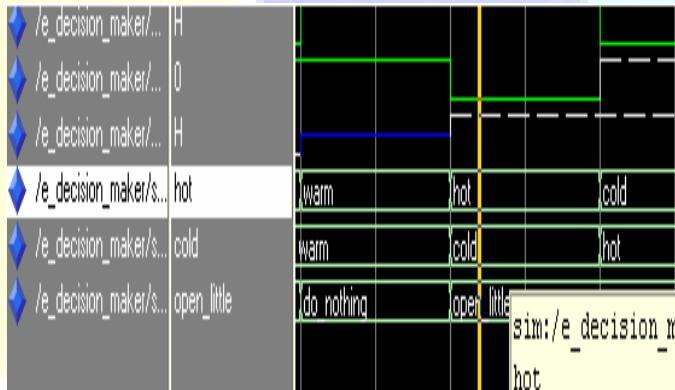


Fig 8(b): Simulation output of Decision Making Circuit

IV. Expected Results:

Result obtained by Fuzzy ART algorithm is compared with the measured output of Fuzzy ART cell by using Tanner Tool and ModelSim.

IV. CONCLUSIONS:

The fuzzy cells present an efficient operation in individual manner, and as part of a complex system. The TMF circuit offers a clear advantage over the other design, since it is able to generate programmable symmetrical and asymmetrical membership function. It also shows a greater flexibility by being constituted by independent cells.

The decision making system not only proved the efficient performance of the proposed cells, it also demonstrated the precision with which a fuzzy system is able to obtain conclusions using rules.

The use of maximum and minimum detection circuit allowed the implementation of fuzzy inference system. Decision making system designed in this work is not only possibility; it also permits the creation of n-rule system with any decision purpose.

The creation of fuzzy VLSI processor that controls the input parameter of the membership function, which represents the knowledge base.

Another action line for the future is the study of the proposed topologies with an analysis perspective of the geometrical change sensitive, mismatches, noise, total harmonic distortion, source noise rejection, in other words the parametric optimization of the design. The design of Bias Column Peripheral Cell; Fuzzy-ART Array Cells along with the various Fuzzy-ART structures is to be done. The Measurement of "Column Bias" Cells, "Weight Currents" will be done. The results of above will be verified with the standard algorithm.

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